



# Status Report of the Laboratory Tests of MIMOSA-26

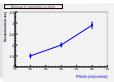
Marc Winter (IPHC/Strasbourg)

on behalf of the IPHC/Strasbourg – IRFU/Saclay collaboration

▷ Work of G.Claus, M.Goffe, G.Dozière, M.Gélin, K.Jaaskelainen and M.Speccht

## OUTLINE

- General features
- Type of tests performed
- Laboratory test results :     ▷ *Analog output*                      ▷ *Discriminated output*  
  ▷ *Zero-suppression logic*    ▷ *Full chain output*
- Next steps
- Summary



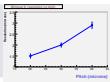
## General Features

### Sensor manufacturing :

- ※ AMS-0.35 fabrication process :  $\sim 15 \mu m$  thin(ck) epitaxial layer
- ※ 3 wafers fabricated (up to 3 additional wafers still available)
- ※ 82 chips per wafer

### Status of sensor delivery :

- ※ 3 wafers back from foundry at CMP in first half of February 2009
- ※ 1/2 wafer (41 sensors) diced and sent to IPHC  $\rightarrow$  received  $\gtrsim$  Feb. 17th
- ※ functionnality tests started in last decade of February 2009
  - $\hookrightarrow$  1st results shown last JRA-1 meeting (early March)
- ※ more recently: 1 wafer sent for thinning to  $\sim 120 \mu m$  and dicing



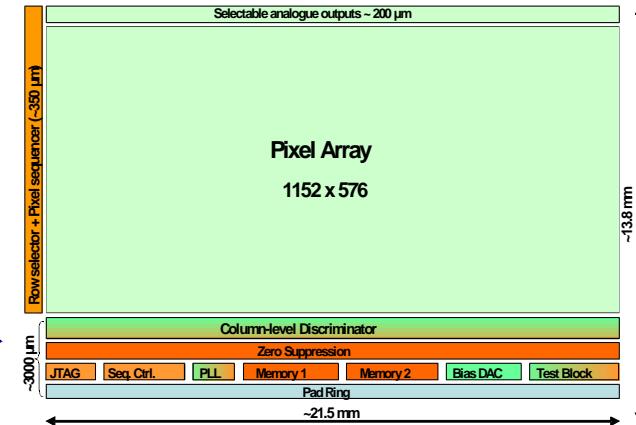
# Prominent Test Features

## Functionnality tests (level 0) :

- \* JTAG → chip alive ? → 1 faulty chip out of 21 bonded
- \* pattern of sensor output (frame header & trailer)

## Analog output characterisation :

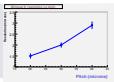
- \* allows characterising pixel matrix and investigating (directly) pixel pbs
- \* activated from sensor side (top) opposite to digital r.o. side (bottom) →
- \* 2 r.o. possibilities : 8 columns at right or sweeping through pixel array
- \* provides pixel noise and uniformity over sensitive area, spots dead or hot pixels, etc.



## Digital output characterisation (4 configurations) :

- \* discriminators alone, i.e. isolated from pixel array (internal voltage injection)
  - ↪ scan threshold uniformity (offset dispersion & temporal noise)  
(also: check possibility to disconnect individual discriminators ≡ disconnect pbtic columns)
- \* discriminators connected to pixel array ⇒ overall FPN and thermal noise
- \* zero-suppression logic and output memories (SUZE-01) alone (JTAG or fired pixel cheater)
- \* test of complete chain : pixel array ⊕ discriminators ⊕ zero-suppresion ⊕ output memories

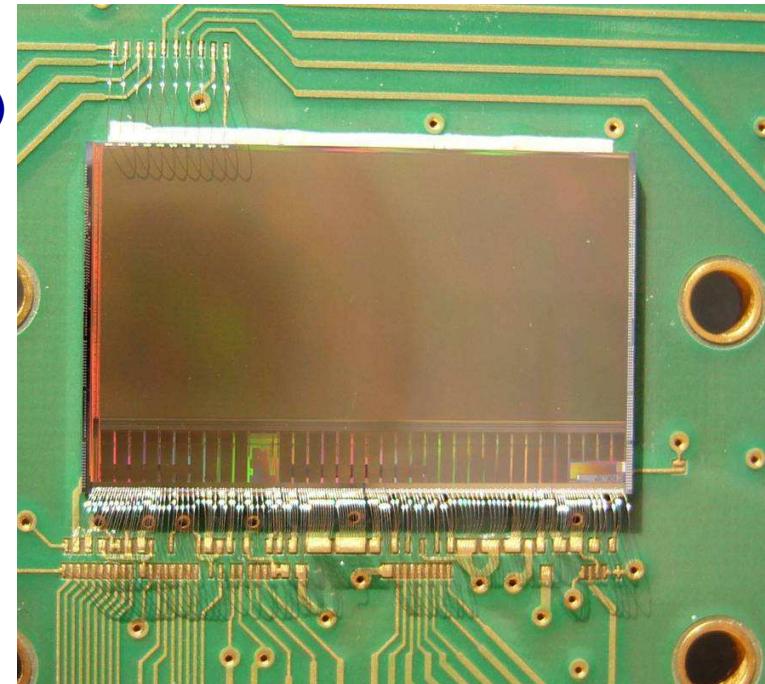
## Test structure of PLL, 8b/10b : data transfer option



## Reminder: Prominent MIMOSA-26 Features

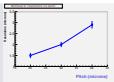
MIMOSA-26  $\equiv$  final sensor for EUDET telescope

- \* MIMOSA-22 (binary outputs) complemented with  $\emptyset$  (SUZE-01)
- \* Active surface : 1152 columns of 576 pixels ( $21.2 \times 10.6 \text{ mm}^2$ )
- \* Pitch :  $18.4 \mu\text{m} \rightarrow \sim 0.7 \text{ million of pixels} \rightarrow \sigma_{sp} \gtrsim 3.5 \mu\text{m}$
- \* Integration time  $\lesssim 110 \mu\text{s} \rightarrow \sim 10^4 \text{ frames / second}$   
 $\Rightarrow$  suited to  $> 10^6 \text{ particles/cm}^2/\text{s}$
- \*  $\emptyset$  in 18 groups of 64 col. allowing  $\leq 9$  "pixel strings" / raw
- \* Sensor full dimensions :  $\sim 21 \times 12 \text{ mm}^2$
- \* Data throughput: 1 output at  $\geq 80 \text{ Mbits/s}$   
or 2 outputs at 40/80 Mbits/s



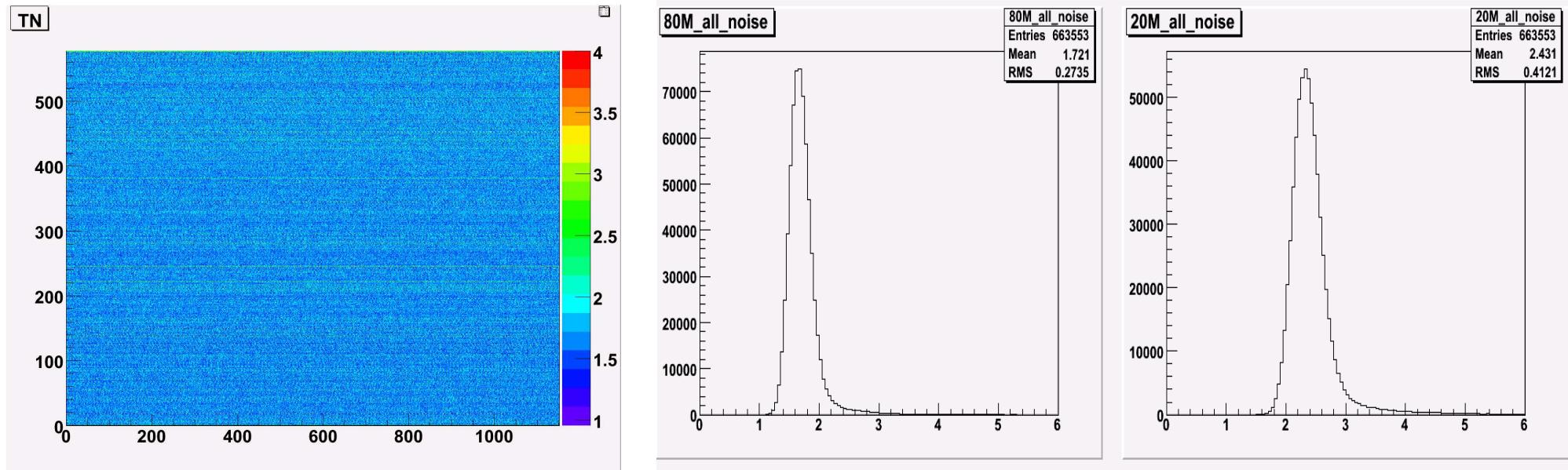
Fabricated in AMS-0.35 technology:

- \* Sensor expected to equip several EUDET BT copies
- \* Architecture is baseline for STAR, CBM and ILC vertex detectors



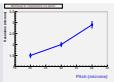
## Analog Output Test Results

### Analog response studied for 8 different sensors :



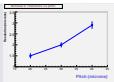
### CCE with $^{55}\text{Fe}$ source : comparison with MIMOSA-22

Cluster size	seed	2x2	3x3	5x5
<b>MIMOSA-26</b>	22 %	55 %	73 %	83 %
<b>MIMOSA-22</b>	22 %	58 %	75 %	86 %



## Analog Output Test Results: Summary

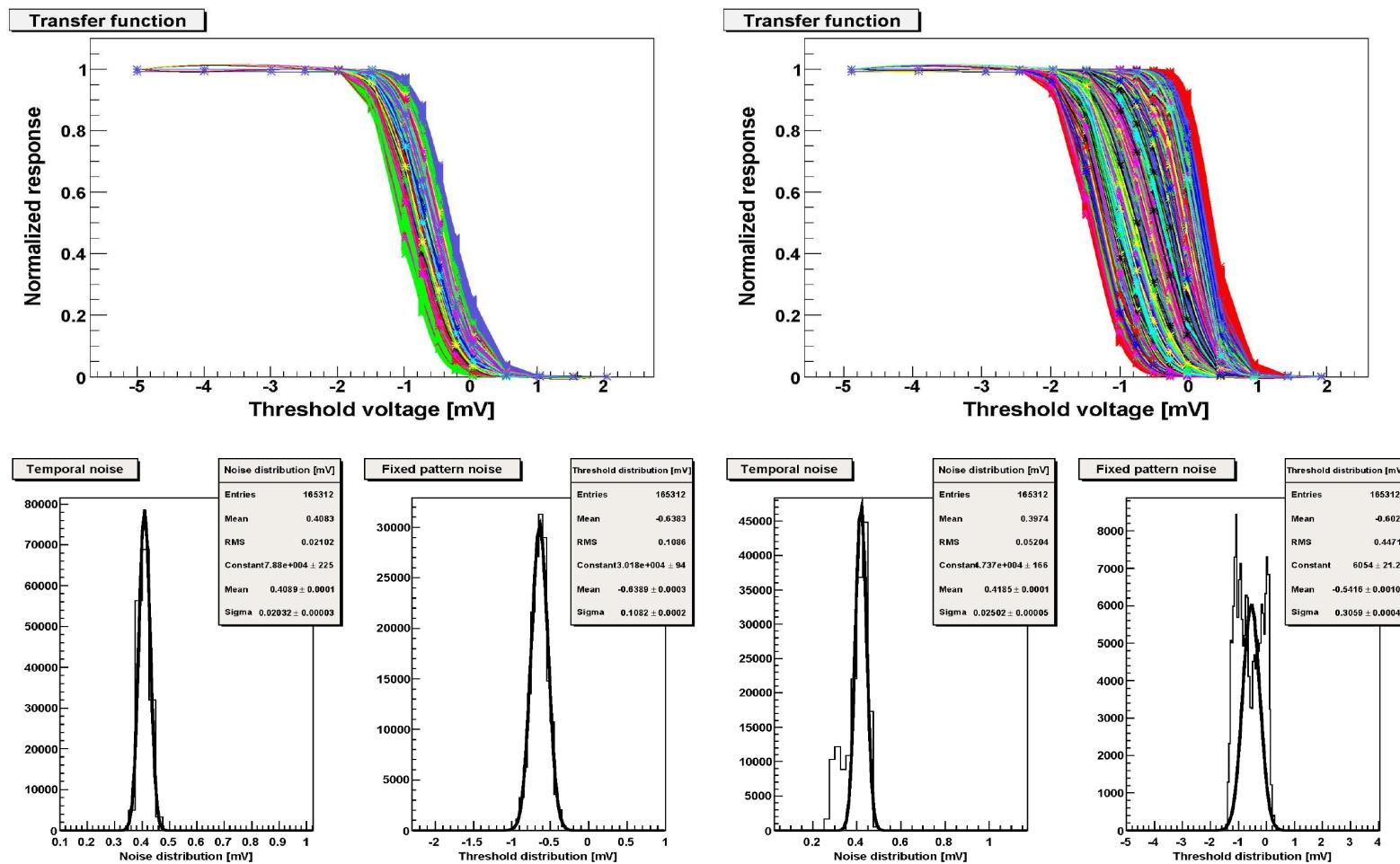
- ※ All pixels are alive (none is dead !)
- ※ Noise is uniform accross the  $2 \text{ cm}^2$  sensitive area
- ※ Satisfactory operation from 80 MHz (nominal) down to 20 MHz (and below)
- ※ Noise and CCE performances are  $\sim$  identical to those of MIMOSA-22
- ※ All 8 sensors exhibit similar behaviours

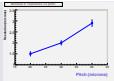


# Isolated Discriminator Output Test Results

## Digital output studied on 9 different sensors :

- \* Noise performance assessed separately for each of the 4 groups of 288 columns (nominal r.o. speed)
- \* Example of sub-array A and C (chip Nr.6)





## Summary of Isolated Discriminator Output Test Results

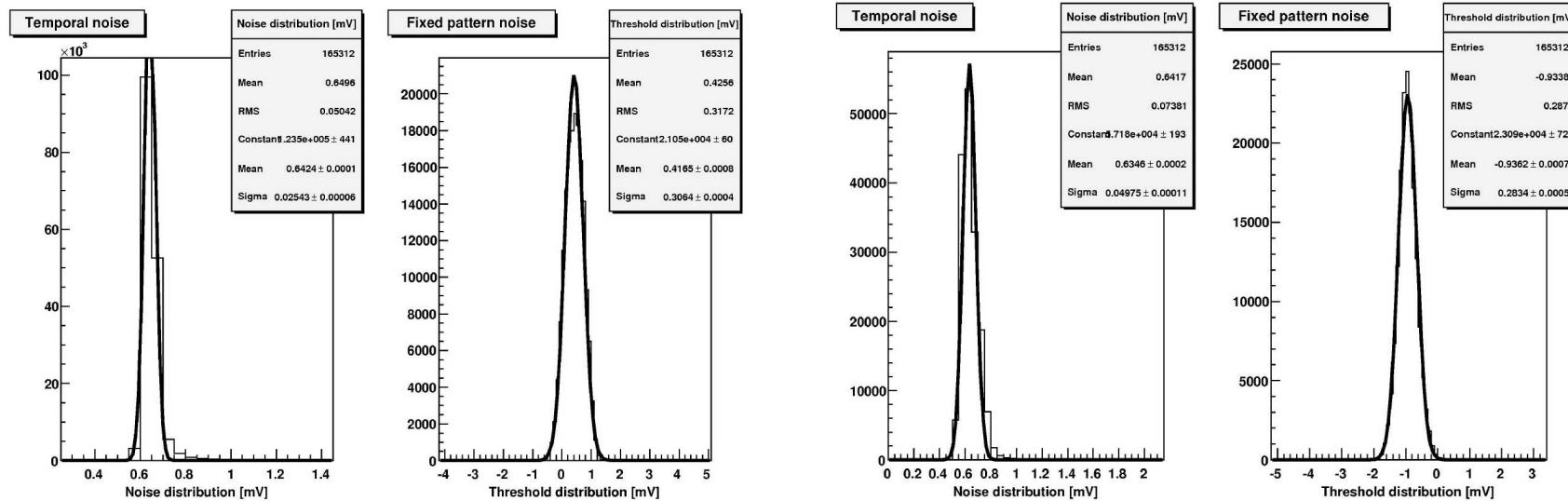
- ✳ Typical value of discriminator thermal noise  $\lesssim 0.3\text{--}0.4 \text{ mV}$
- ✳ Discriminator FPN  $\lesssim 3 \text{ e}^- \text{ ENC}$  (i.e. 0.15 mV)
- ✳ Results are  $\sim$  identical to MIMOSA-22 values in sub-array A,  
and slightly worse in sub-array B, C, (D)  
  
 $\Rightarrow$  **All discriminators are operational at nominal speed** (and below )



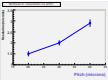
# Analog $\oplus$ Discriminated Output Test Results

## Digital output studied on 9 (resp. 4) different sensors at 80 (resp. 20) MHz :

- \* Noise assessed separately for each group of 288 columns, at nominal r.o. speed & below  
↪ example of sub-array A and C of chip-6 :



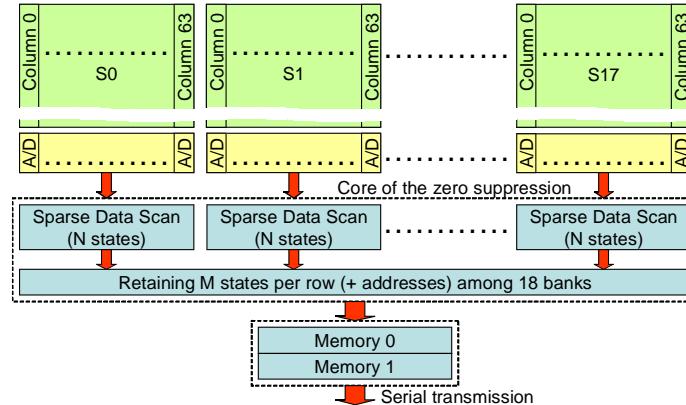
- \* Typical value of total temporal noise  $\sim 0.6\text{--}0.7$  mV
  - \* Typical value of total FPN noise  $\sim 0.3\text{--}0.4$  mV
  - \* Results are  $\sim$  identical to MIMOSA-22 values ( $N \lesssim 12\text{--}13$  e<sup>-</sup> ENC)
  - \* 80  $\rightarrow$  20 MHz: pixel noise  $\nearrow$  & discri. noise  $\searrow \Rightarrow$  mild overall change
- ⇒ Array of 660,000 pixels coupled to 1152 discriminators works  $\sim$  as expected



# Zero-Suppression and Output Memories Test Results



## Conclusion of the Mimosa 26 Ø Core test result

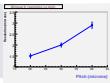


- The pixel array has 575 rows x 1152 columns.
- Zero suppression is based on row by row sparse data scan readout
- Functionality tests:
  - ↳ Encoding addresses (line, column) of the hit function (systematic and randomly),
  - ↳ Encoding of the states (0 to 9 STATES) in all column positions of the 18 banks (systematic and randomly),
  - ↳ Encoding of the shape of the state: 1 to 4 consecutive pixels (systematic and randomly),
  - ↳ Checking of the continuity between blocks,
  - ↳ Encoding patterns with more than 9 states detected (overflow)
  - ↳ Working Frequency range: 10 MHz to 115 MHz.
  - ↳ Output modes: 2 outputs 80 MHz, 1 Output 80 MHz, 2 outputs 40 MHz.
- 3 patterns tested 7 millions times without errors
- Robustness test: 199 frames x 10 000 random patterns test at 80 MHz without errors.

26/05/2009

IPHC G.Doziere & Team Test

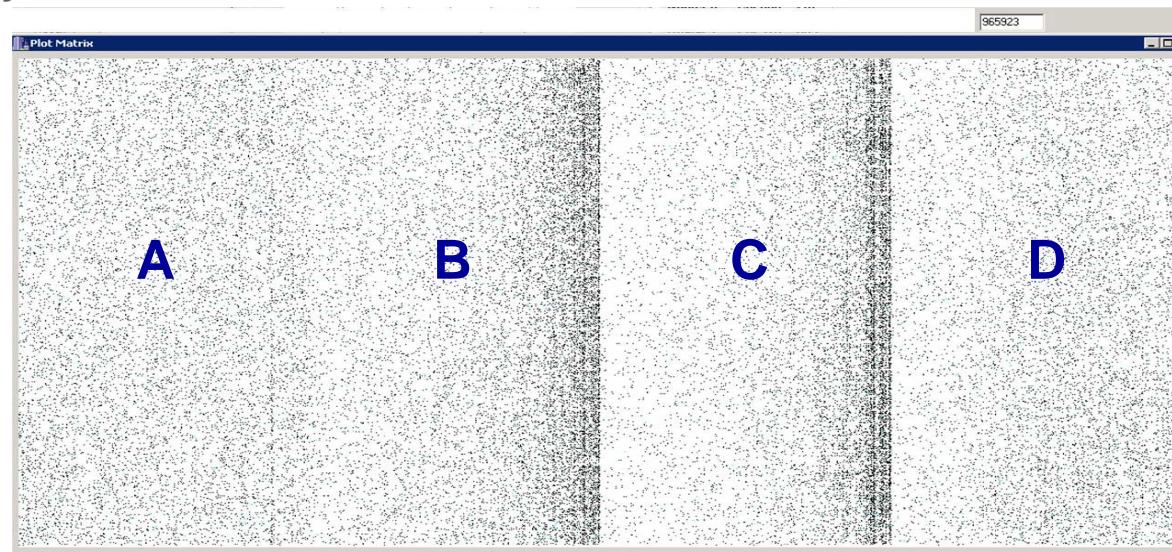
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## Full Chain Test Results

### ■ Full chain signal delivery studied on several different sensors :

Ex: Chip-6 output  
for 5 N threshold  
(10,000 frames )

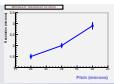


- \* Fake hit rate due to pixel noise fluctuations at 80 MHz
- \* Varying the operation T from +20°C to +40°C  $\rightarrow$  essentially no change
- \* Multi-hit emulation of pixel array checked to generate the right memory output pattern

Discri. threshold	4 N	5 N	5.5 N	6 N	8 N	10 N
$N_{pix} > \text{threshold } (10^{-4})$	$\lesssim 8$	$\sim 1.5$	$\sim 1$	0.5	0.1	0.03

### ■ Running 3 sensors simultaneously :

- \* Test on frame header and trailer during 14 hours ( $40 \cdot 10^6$  frames without error)
- \* Test on zero-supp. data (1 emulated hit/line) running during 14 hours ( $2.3 \cdot 10^6$  frames without error)

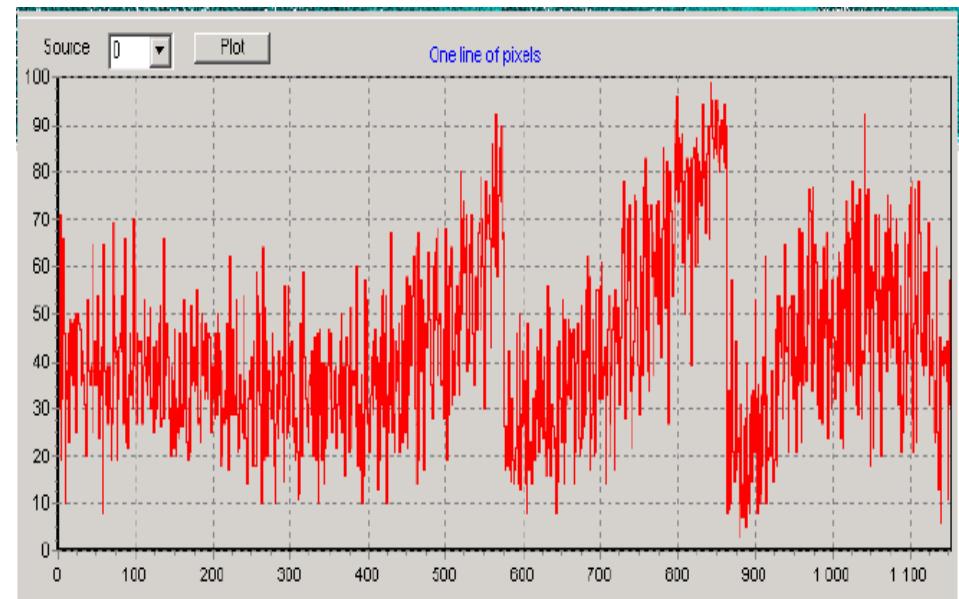
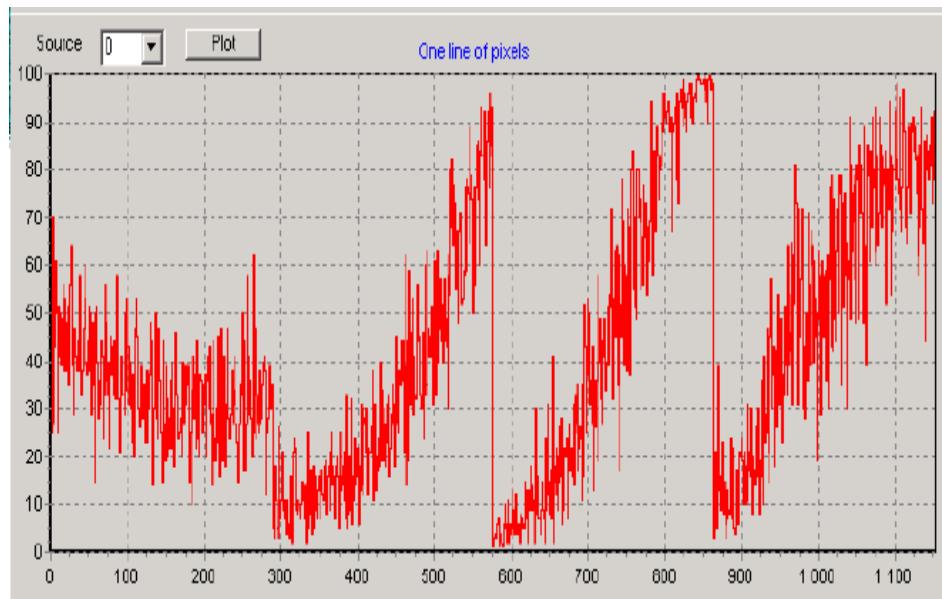


## - Dispersion of Discriminator Thresholds

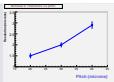
### ■ Threshold scan of discriminators :

◊ Disconnected from pixel array

◊ Connected to pixel array



⇒ Dispersion seems mitigated when connecting the discriminators to pixel array



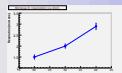
## Summary of Imperfections Observed

### Observed anomalies :

- \* discriminator threshold non-uniformity  $\Rightarrow$  understood: put threshold  $\gtrsim 5.5$  N in group B, C, (D )
- \* incomplete cluster encoding in raw 576  $\Rightarrow$  understood
- \* structures ("crocodile skin" - G.C.) in discri. threshold scan  $\Rightarrow$  under study
  - ↪ discri. steering feature ?
- \* r.o. frequency dependence of pixel temporal N (calib. peak)  $\Rightarrow$  due to integrated test  $\mu$ circuitry ?
- \* etc.

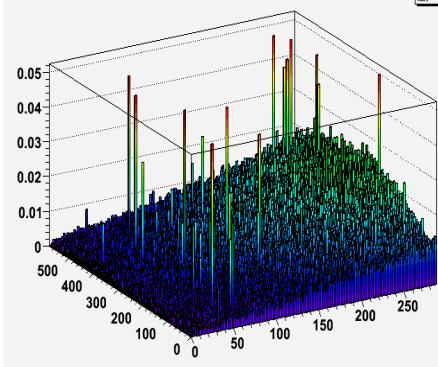
### Comments :

- \* only modest disturbance expected on beam telescope operation
- \* part of anomalies suspected to come from too weakly optimised measurement procedures
- \* their study is essentially motivated by the design plans of coming sensors which are derived from MIMOSA-26 : STAR, CBM, ILC

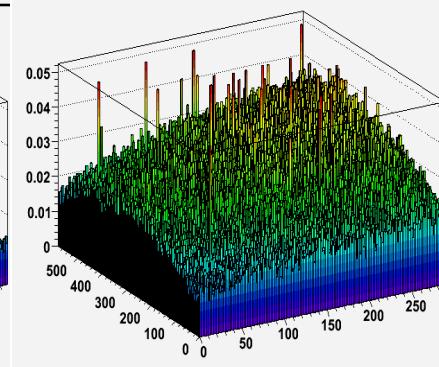


## Illumination with $^{55}\text{Fe}$ Source

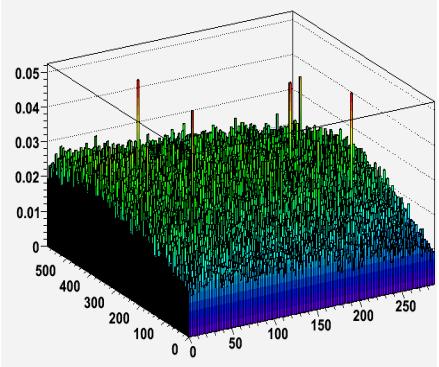
Sub-array 0 - threshold 0



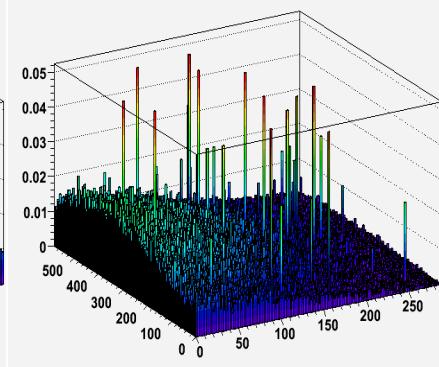
Sub-array 1 - threshold 0



Sub-array 2 - threshold 0

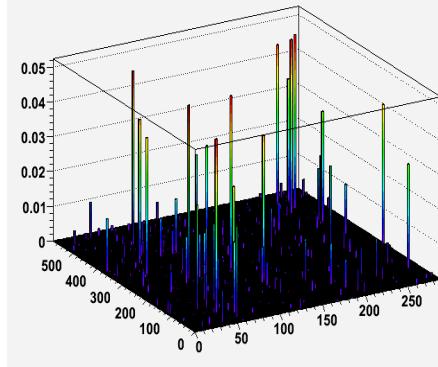


Sub-array 3 - threshold 0

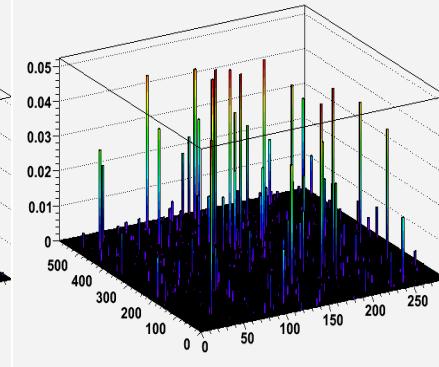


Avec source

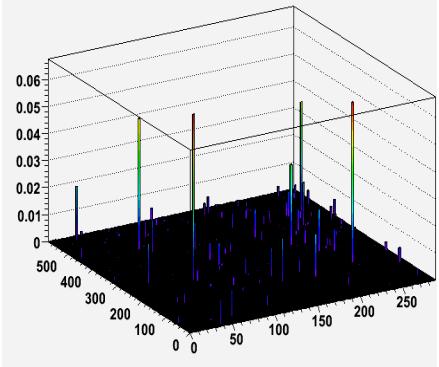
Sub-array 0 - threshold 0



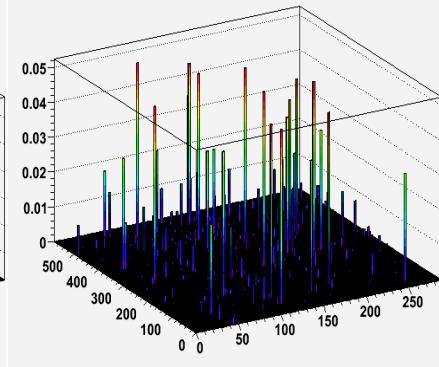
Sub-array 1 - threshold 0



Sub-array 2 - threshold 0

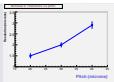


Sub-array 3 - threshold 0



sans source

Chip 8  
Frequence 80 MHz  
coupure sur bruit = 10

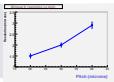


## ■ Complement laboratory tests :

- \* Performances of  $50 \mu m$  thin sensors
- \* Improve understanding of anomalies (for MIMOSA-26 extensions )
- \* Operate 6 sensors synchronously
- \* Radiation tolerance ?

## ■ Beam tests:

- \* Period: Septembre 2009 at CERN-SPS (T4-H6)
- \* Objectives:
  - ≈  $N, \epsilon_{eff}$ . vs fake rate for various discriminator thresholds
  - ≈  $\sigma_{SP}$ , cluster characteristics for various discriminator thresholds
  - ≈ synchronous running of 6 sensors, ...



# SUMMARY

## MIMOSA-26 qualification:

- ≈ sensor has been quite extensively studied in lab (including synchronous operation of 3 chips)
- ≈ MIMOSA-22 performances reproduced on complete sensitive surface
- ≈ fabrication yield  $\gtrsim 90\%$
- ≈ all imperfections found are affordable (will be corrected in sensors derived from MIMOSA-26)  
⇒ **Overall performances satisfy specifications ⇒ sensor validated for beam tests**

## What remains to be done

- ≈ complementary lab tests: yield estimate for thinned sensors, operation of 6 sensors, etc.
- ≈ beam tests in Septembre :  $\epsilon_{eff}$ , fake rate and  $\sigma_{SP}$  vs discri. threshold



# Integration Tests : Steering & Readout of N x Mimosa 26

Pattern generator

( Tektron DG2020A )



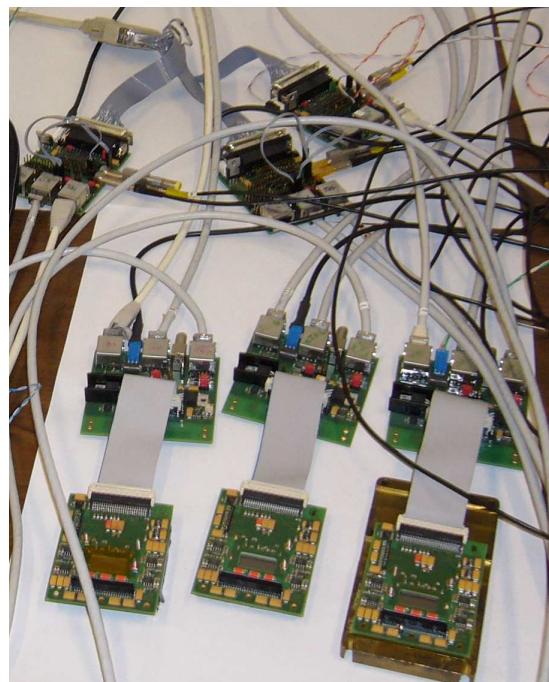
- Clock X 3
- Start X 3

DAQ NI

PXI 6562 Board



- Clock & Sync X 1
- Data (D0,D1) X 3



3 x Mimosa 26

Readout D0, D1 @ 80 MHz

11/06/2009

EUDET Meeting, Geneva June 2009

IPHC - DRS Gilles CLAUS & Test Team

1/1

## Goal / Method

- ▶ How to run more than one Mimosa 26 on a Telescope like DAQ system ?

- ▶ How to start all Mimosa 26 at the same time ?
- ▶ Will they keep synchronization over a long run ?
- ▶ Trigger handling

- ▶ How to perform this test ?

- ▶ Star distribution of clock and external Start to all Mimosa 26
- ▶ External Start source synchronized / CLK falling edge
- ▶ Acquisition of all Mimosa 26 by the same DAQ board ( NI PXI 6562 )

## Tests Done / Results

- ▶ Test on Header & Trailer with 3 Mimosa 26

- ▶ 40 10<sup>6</sup> frames without error → Test stopped after ~ 14H00

- ▶ Test on ZS data ( one emulated hit / line ) with 3 Mimosa 26

- ▶ 2,3 10<sup>6</sup> frames without error → Test stopped after ~ 14H00

- ▶ Next steps ...

- ▶ Test with six Mimosa 26

- ▶ Trigger handling



## Commercial DAQ board : NI Flex RIO ?

### NI FlexRIO – Custom I/O for LabVIEW FPGA and PXI

#### NI PXI-795xR NEW!

- Virtex-5 FPGA-programmable with the LabVIEW FPGA Module
- Up to 128 MB onboard DDR2 DRAM
- Access to 132 single-ended I/O lines, configurable as 66 differential pairs
- Customizable I/O with the NI FlexRIO Adapter Module Development Kit (MDK)
- 100 MHz digital I/O with the NI 6581 adapter module
- 3 DMA channels for high-speed data streaming

##### Operating Systems

- Windows Vista/XP/2000
- LabVIEW Real-Time

##### Required Software

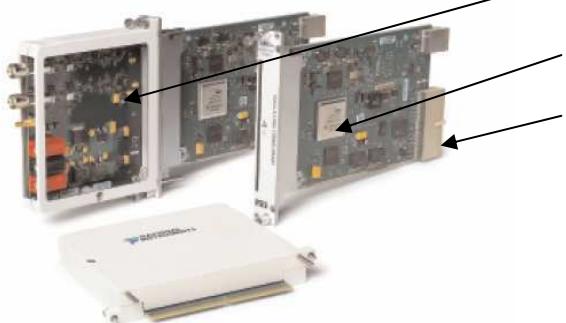
- LabVIEW
- LabVIEW FPGA Module
  - LabVIEW code compiler for FPGAs
  - Emulated debugging mode

##### Recommended Software

- LabVIEW Real-Time Module

##### Driver Software (included)

- NI-RIO



Model	Bus/Form Factor	FPGA	FPGA I/O	Onboard Memory (DRAM)
PXI-7951R	PCI	Virtex-5 LX30	66 differential or 132 single-ended	0 MB
PXI-7952R	PCI	Virtex-5 LX50	66 differential or 132 single-ended	128 MB
PXI-7953R	PCI	Virtex-5 LX85	66 differential or 132 single-ended	128 MB
PXI-7954R	PCI	Virtex-5 LX110	66 differential or 132 single-ended	128 MB

Table 1. NI FlexRIO FPGA Modules

### Future ?

- PXIE ? 250 MB/s / lane ... X 1, 2, 4, 8, 12, 16, 32 → 6 GB/s ...

- Can't be handled by software ...
- Writing to disk + % of monitoring by software

- Fast serial links Gb/s

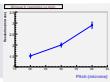
- Direct handling on FPGA ?
- User HW on Adaptater Module

### Current Status

- 66 Differential inputs
- User defined Adaptator Module
- User defined on-board fw ( deserialisation )
- PXI bus → Average ~ 60 MB/s
- 1 Mi26 plane @ 10 kframe/s → ~ 25 MB/s
- 4 Planes ~ 100 MB/s → 60 % of full speed
- 6 Planes ~ 150 MB/s → 40 % of full speed

### Cost ?

- PXI-7951R ( No RAM ) ~ 2,8 K€
- PXI-7952R ( 128 MB RAM ) ~ 3,7 K€
- Adaptator module SE 100 MHz ~ 1 K€
  - LVDS foreseen for end of summer
- PXIE Crate + CPU ~ 8 K€
- Adaptater Module Development Kit ~ 4,6 K€
  - Overhead of 4,6 K € ( CAD files etc ... )
  - ~ 60 € / enclosure



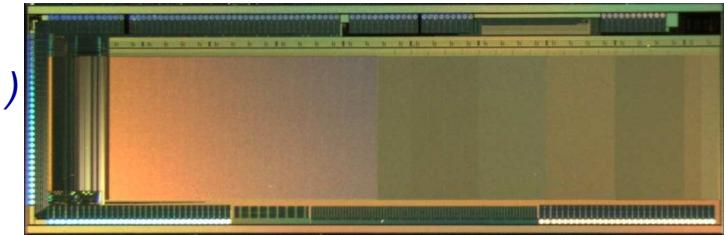
## Performances of MIMOSA-22

MIMOSA-22 : ◊ fabricated in 2007/08 (coll. with IRFU/Saclay)

◊ 136 col. of 576 pixels ( $18.4 \mu\text{m}$  pitch, integrated CDS )

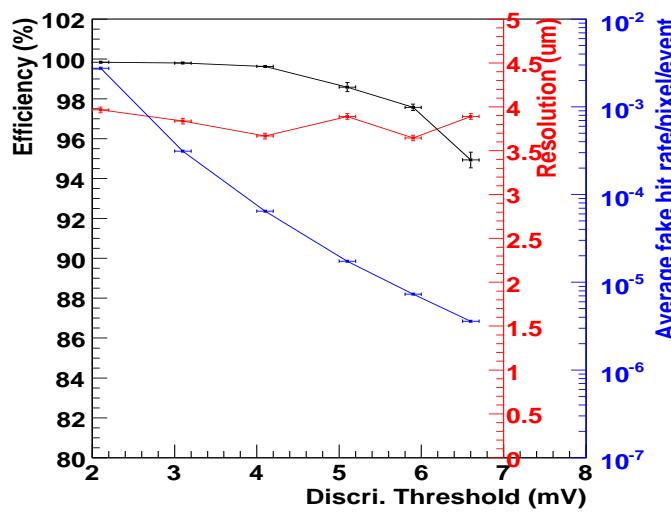
◊ 128 col. ended with an integrated discriminator

◊ integrated JTAG controller

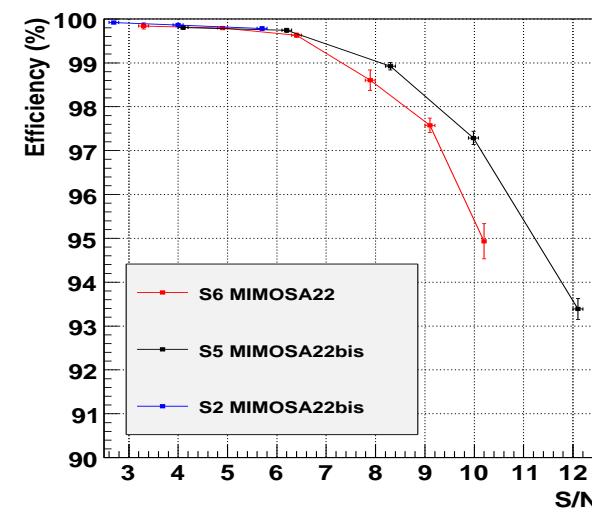


Tests at CERN-SPS ( $\sim 120 \text{ GeV } \pi^-$ ) in 2008 → results of different sub-arrays

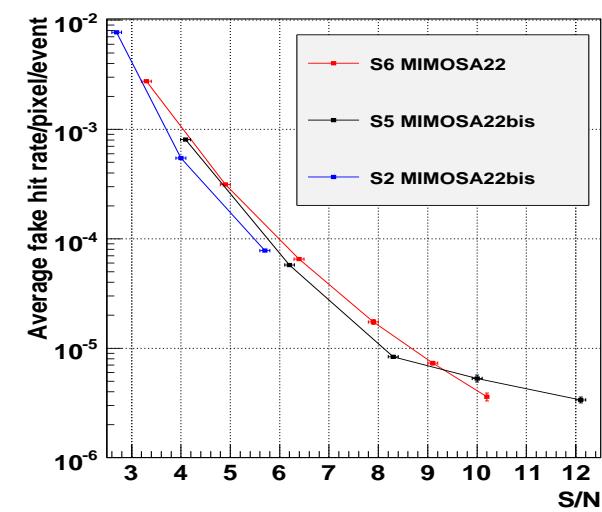
M22 digital S6. Efficiency, Fake rate and Resolution



S6 M22, S5 M22bis & S2 M22bis digital Efficiency



M22bis digital fake hit rate



►►► Architectures of pixel (integrated CDS ) and of full chain made of  
"columns ended with integrated discreti. " validated at real scale